REMARKS

Claims 1-15 and 27-37 are pending in the application with claims 1, 10, 13, 28, and 29 amended herein.

Claims 1-5, and 9 stand rejected under 35 U.S.C. 102(e) as being anticipated by Yamanishi (U.S. Patent No. 6,307,730). Applicant requests reconsideration.

Amended claim 1 sets forth a capacitor fabrication method that includes, among other features, forming undoped, rugged polysilicon over a substrate, forming a first capacitor electrode over the rugged polysilicon, forming a capacitor dielectric layer over the first electrode and over the rugged polysilicon, and forming a second capacitor electrode over the dielectric layer and over the rugged polysilicon. Page 3 of the Office Action alleges that Yamanishi discloses every limitation of claim 1. However, Applicant asserts that Yamanishi fails to disclose forming a capacitor dielectric layer over rugged polysilicon or forming a second capacitor electrode over rugged polysilicon.

Review of Yamanishi does not reveal disclosure or suggestion of forming capacitor insulating layer 14 or upper capacitor electrode 15 over HSG polycrystalline silicon layer 21a. Instead, column 4, lines 49-55 and elsewhere throughout Yamanishi expressly require removal of all of HSG polycrystalline silicon layer 21a prior to forming capacitor insulating layer 14 and upper capacitor electrode 15. At least for such reason, Yamanishi does not anticipate claim 1.

Further, it is clear from Yamanishi that modification thereof by leaving in place HSG polycrystalline silicon layer 21a shown in Fig. 3H would frustrate the intended purpose of increasing the capacitor capacity stated at least in column 1, lines 34-47. Accordingly, no motivation can be considered to exist to modify Yamanishi by forming capacitor insulating layer 14 or upper capacitor electrode 15 over HSG polycrystalline silicon layer 21a. Claim 1 is thus additionally patentable over Yamanishi.

Claims 2-5 and 9 depend from claim 1 and are not anticipated at least for such reason as well as for the additional limitations of such claims not disclosed. In the context of the Yamanishi novelty rejection, page 4 of the Office Action discusses claims 10, 27, and 28. However, it is not clear whether such claims are rejected as being anticipated by Yamanishi. The page 4 text refers to Figs. 18, 19, 20, and 22 that do not exist in Yamanishi. Accordingly, Applicant assumes that the discussion pertaining to claims 10, 27, and 28 is unintentionally included with the Yamanishi novelty rejection and Applicant does not respond herein to such grounds for rejection.

Claims 6-8, 10-15, and 27-37 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Yamanishi as applied to claims 1-5, and 9 above in view of Fukuzumi et al. (U.S. Patent No. 6,222,722), Sneh et al. (U.S. Patent No. 6,551,399) and Raaijmakers et al. (U.S. Patent No. 6,780,704). Applicant requests reconsideration.

Claims 6-8 and 27 depend from claim 1 the subject matter of which is discussed above. Fukuzumi, Sneh, and Raaijmakers do not disclose or

suggest and are not alleged to disclose or suggest the subject matter absent from Yamanishi. A combination of references cannot be considered to disclose or suggest subject matter that is absent from each reference. Accordingly, claims 6-8 and 27 are patentable over the cited combination.

Pages 6-7 of the Office Action include a discussion of claim 27 and allege, referring to Figs. 30-34 of Fukuzumi, that such reference discloses undoped, rugged polysilicon. In its Response to September 27, 2004 Office Action, Applicant previously established on pages 8-10 that polysilicon film 51 of Fukuzumi does not disclose or suggest undoped rugged polysilicon. Applicant herein incorporates by reference the portions of such previous Response that are pertinent to the allegations on pages 6-7 of the Office Action.

Amended claim 10 sets forth a capacitor fabrication method that includes, among other features, forming a layer of polysilicon over the sides and bottom of an opening in an insulative layer, converting at least some of the polysilicon layer to undoped hemispherical grain polysilicon, conformally forming a first capacitor electrode on and in contact with the hemispherical grain polysilicon, forming a capacitor dielectric layer on the first electrode and over the hemispherical grain polysilicon, and forming a second capacitor electrode over the dielectric layer and over the hemispherical grain polysilicon. As may be appreciated from the discussion above regarding the deficiencies of Yamanishi as applied to claim 1, Yamanishi fails to disclose or suggest forming a capacitor dielectric layer and a second capacitor electrode

over the hemispherical grain polysilicon. Fukuzumi, Sneh, and Raaijmakers do not remedy the deficiencies of Yamanishi. At least for such reason, claim 10 is patentable over the cited combination. Claims 11, 12, 14, 15, 30, and 31 depend from claim 10 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested.

Amended claim 13 sets forth a capacitor fabrication method that includes, among other features, forming a layer of polysilicon over the sides and bottom of an opening in an insulative layer, converting at least some of the polysilicon layer to hemispherical grain polysilicon, chemisorbing a first capacitor electrode on and in contact with the hemispherical grain polysilicon, forming a capacitor dielectric layer on the first electrode and over the hemispherical grain polysilicon, and forming a second capacitor electrode over the dielectric layer and over the hemispherical grain polysilicon. As may be appreciated from the discussion above regarding the deficiencies of Yamanishi as applied to claim 1, Yamanishi fails to disclose or suggest forming a capacitor dielectric layer and a second capacitor electrode over the hemispherical grain polysilicon. Fukuzumi, Sneh, and Raaijmakers fail to remedy the deficiencies of Yamanishi. Accordingly, claim 13 is patentable over the cited combination. Claims 32 and 33 depend from claim 13 and are patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested.

Amended claim 28 sets forth a capacitor fabrication that includes, among other features, forming a capacitor dielectric layer and a second

capacitor electrode over hemispherical grain polysilicon. As may be appreciated from the discussion above regarding the deficiencies of Yamanishi as applied to claim 1, Yamanishi fails to disclose or suggest every limitation of claim 28. Fukuzumi, Sneh, and Raaijmakers fail to remedy the deficiencies of Yamanishi. Accordingly, claim 28 is patentable over the cited combination. Claims 34 and 35 depend from claim 28 and patentable at least for such reason as well as for the additional limitations of such claims not disclosed or suggested.

Amended claim 29 sets forth a capacitor fabrication method that includes, among other features, forming a capacitor dielectric layer and a second capacitor electrode over hemispherical grain polysilicon. As may be appreciated from the discussion above regarding the deficiencies of Yamanishi as applied to claim 1, Yamanishi fails to disclose or suggest every limitation of claim 29. Fukuzumi, Sneh, and Raaijmakers fail to remedy the deficiencies of Yamanishi. Accordingly, claim 29 is patentable over the cited combination. Claims 36 and 37 depend from claim 29 and are patentable at least for such reasons as well as for the additional limitations of such claims not disclosed or suggested.

Applicant herein establishes adequate reasons supporting patentability of claims 1-15 and 27-37 and requests allowance of all pending claims in the next Office Action.

Respectfully submitted,

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